Appl. No. 10/708,426 Amdt. dated March 22, 2005 Reply to Office action of February 01, 2005

REMARKS/ARGUMENTS

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajagopalan et al. (U.S. 6,656,840 B2).

Response:

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Claim 1 was rejected under 35 U.S.C. 102(e), for reasons of record that can be found on pages 2-3 in the Office action identified above, which is Part of Paper No./Mail Date 20050128.

To overcome this 102 rejection, Claim 1 has been amended as set forth in the above AMENDMENT section. The limitation in Claim 5 has been added into Claim 1. Claim 5 is accordingly canceled by this amendment. No new matter is introduced.

The Applicants believe that none of the prior art records teach a method for forming damascene interconnect structure with a bi-layer capping film, comprising the following steps:

providing a semiconductor wafer;

depositing a dielectric layer over the semiconductor wafer, the dielectric layer having a main surface and a damascened recess on the main surface;

depositing a copper layer in the damascened recess and to fill the damascened recess;

performing a chemical mechanical polishing process to polish the copper layer such that the copper layer has an exposed upper surface substantially co-planar with the main surface of the dielectric layer; and

capping the exposed upper surface with a bi-layer capping film consisting of a lower HDPCVD silicon nitride layer and an upper oxygen doped silicon carbide layer, as limited by amended Claim 1.

25 Reconsideration of the amended Claim 1 is therefore politely requested.

As Claims 2-4, and 6 are dependent upon Claim 1, they should be allowable if Claim 1 is allowed. Reconsideration of Claims 2-4, and 6 is therefore politely requested.

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Applicants respectfully request that a timely Notice of Allowance be issued in this case.

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Sincerely yours,

Wenton Hars

Date: March 22, 2005

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